## **IN THE DRAWINGS**

Please amend Figure 1 as marked.

## **IN THE CLAIMS**

Please amend the claims as follows:

(Amended) A processor comprising:

a first instruction set engine to process instructions having a first word size; a second instruction set engine to process instructions having a second word size, the second word size being different than the first word size;

a mode identifier;

a plurality of floating-point registers shared by the first instruction set engine and the second instruction set engine; and

a floating-point unit coupled to the floating-point registers, the floating-point unit processing an input responsive to the mode identifier to produce an output.

11. (Amended) The method of Claim 10 wherein the input is comprised of at least one operand and at least one operator; wherein detecting comprises examining the at least one operand to determine whether any of the operands correspond to the token; and wherein checking comprises examining a mode identifier to determine whether the processor is in the first mode or the second mode.

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